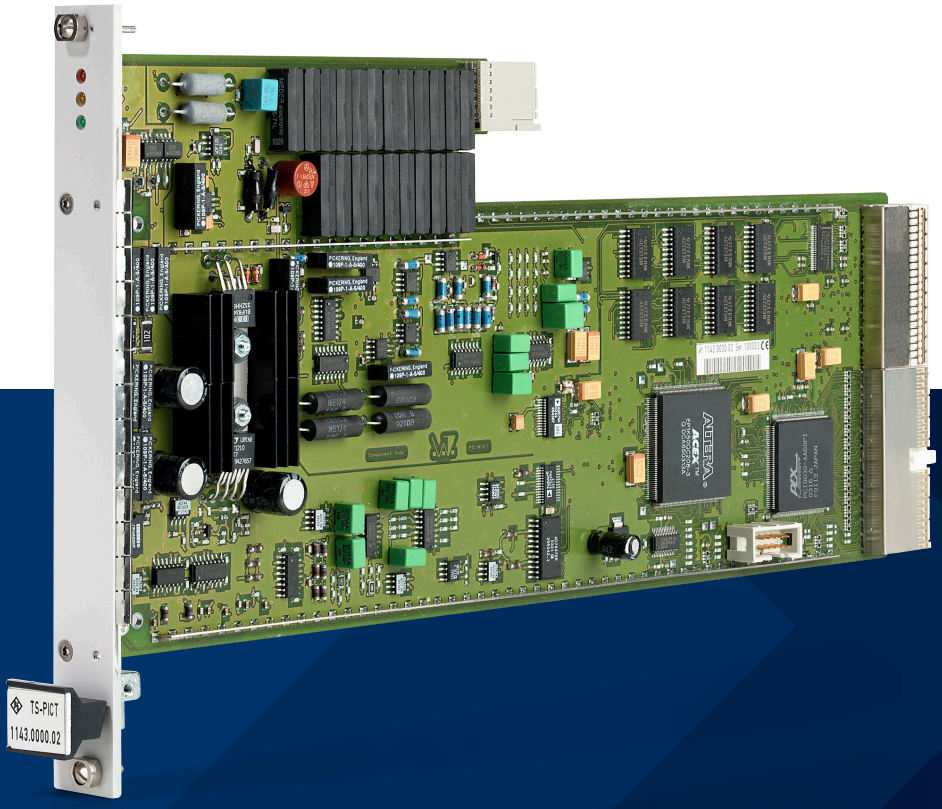
R&S®TS-ICT
IN-CIRCUIT TEST OPTION FOR R&S®TSVP

Using R&S®TS-PSAM, R&S®TS-PICT, R&S®TS-PMB, R&S®TS-PSU and R&S®EGTSL software



Product Brochure
Version 02.00

ROHDE&SCHWARZ
Make ideas real

AT A GLANCE

Continuing the R&S®TSVP product family's philosophy of scalability and flexibility, a modular and cost-effective in-circuit test (ICT) platform can also be easily created using hardware and software from the R&S®TSVP product portfolio.

Key facts

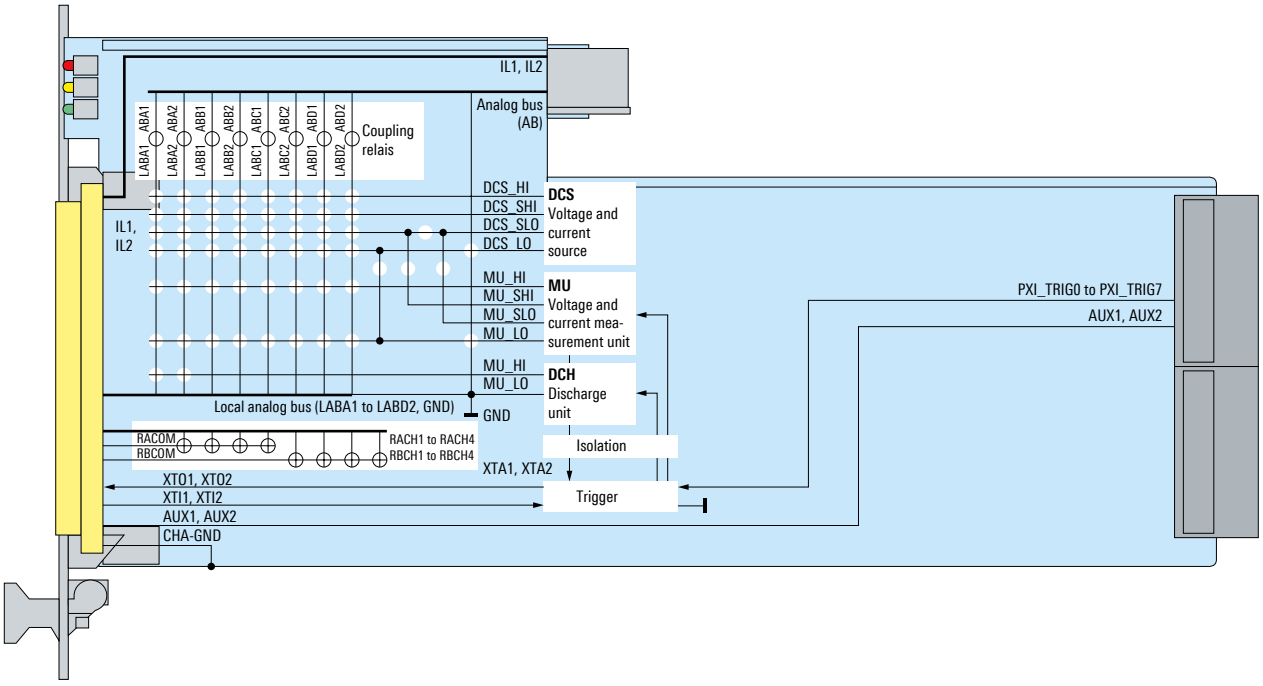
- Complete analog in-circuit measurement unit with R&S®TS-PSAM, R&S®TS-PSU and R&S®TS-PICT
- Test of R, L, C, diodes, transistors, parallel R-C
- Guarded resistor measurements (3-, 4-, 6-wire)
- Guarded impedance measurements (3-, 4-, 6-wire)
- Measurement frequencies 100 Hz, 1 kHz, 10 kHz for impedance tests
- Low stimulus voltage for isolation of diodes and ICs
- Test system based on CompactPCI, PXI and CAN
- Up to 300 tested parts per second
- Automatic test generator with circuit analysis and testability check
- Standard interface for CAD data import
- Easy-to-use enhanced generic test software library (EGTSL) environment for in-circuit test debugging
- Up to 990 test pins in single-chassis
- Up to 2430 test pins in dual-chassis together with R&S®PowerTSVP solution

Product introduction

The R&S®TS-ICT option provides a wide variety of standardized test methods and combinations. To meet each customer's requirements, the classic analog ICT can be merged with all functional tests (FCT) offered by the R&S®TSVP family as well as with the entire spectrum of products from the PXI and cPCI market.

The R&S®TS-ICT option is based on the R&S®TS-PSAM, R&S®TS-PSU and R&S®TS-PICT modules. Each module takes up only one slot in the PXI frame. The R&S®TS-PICT expands the R&S®TS-PSAM analog source and measurement module to provide fully analog ICT capability. Together with the R&S®TS-PSU power supply module, Zener voltage and transistor beta measurements are possible. In ICTs and FCTs, the DUT's test pins are routed via the R&S®TS-PMB switch matrix module and the analog bus to the measurement and stimulus units. Therefore, the same test pins can be used for ICTs and FCTs.

Functional block diagram of the R&S®TS-PSAM analog source and measurement module



Typical applications

Since the ICT functionality is divided into different modules, the modular ICT option can be precisely configured to the customer's requirements. Applications may vary from an FCT enhancement to a classic analog ICT solution.

The ICT expansion provides the following benefits, especially for the FCT:

- A contact test checks whether the contacts with the DUT (wiring test) are functioning properly
- A shorts test prevents the DUT or the test system from being destroyed during power-up
- A continuity test detects open signal paths

When the modular ICT option is used, even a full ICT system can be configured, thus providing the following features:

- Automated test generation
- Highest flexibility in terms of scalability and functionality
- Excellent test speed
- State-of-the-art graphics based debugging environment

In addition, the implementation of the industry standards PXI and CompactPCI ensures that FCT methods can be added regardless of vendor.

Hardware

For ICTs, the following measurement tasks are performed by the R&S®TS-PSAM:

- Discharge of capacitors and printed boards
- Contact test
- Shorts test
- Continuity test
- 2-wire and 4-wire resistance measurements (DC)
- Measurement hardware for system self-test

In addition, the R&S®TS-PSAM covers essential FCT requirements:

- Current/voltage measurement
- Data acquisition (i.e. waveform recording)
- Trigger/clock generation

In conjunction with the R&S®TS-PICT, guarded measurements can also be performed:

- Resistor, capacitor, inductor (AC) tests
- 3-, 4- and 6-wire resistance (DC) and impedance measurements (AC)
- Diode and transistor tests

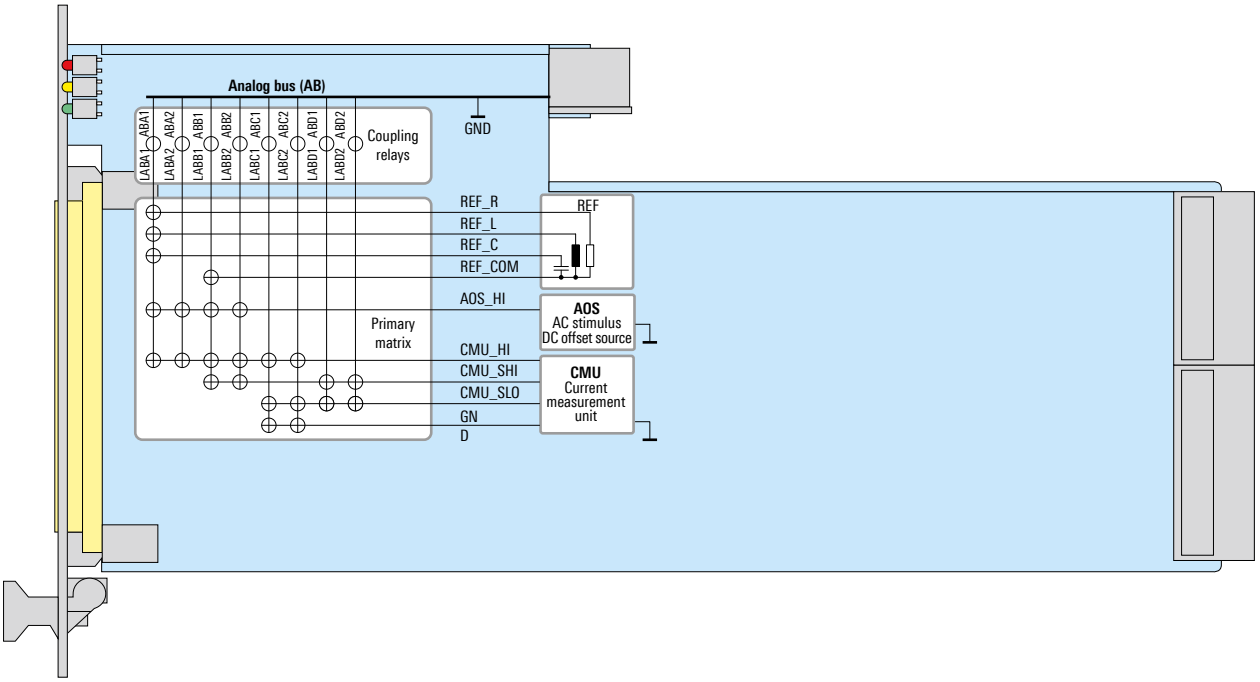
Together with the R&S®TS-PSU or R&S®TS-PSU12 power supply/load module, Zener voltage and transistor beta measurements are possible.

Wiring the adapter is simplified by the full matrix of the R&S®TS-PMB switching matrix module in the case of 2-wire and 4-wire techniques. This module is controlled by the controller area network (CAN) bus, which has already proven itself to be a rugged bus system in the automotive market. The pin count is scalable in steps of 90 pins.

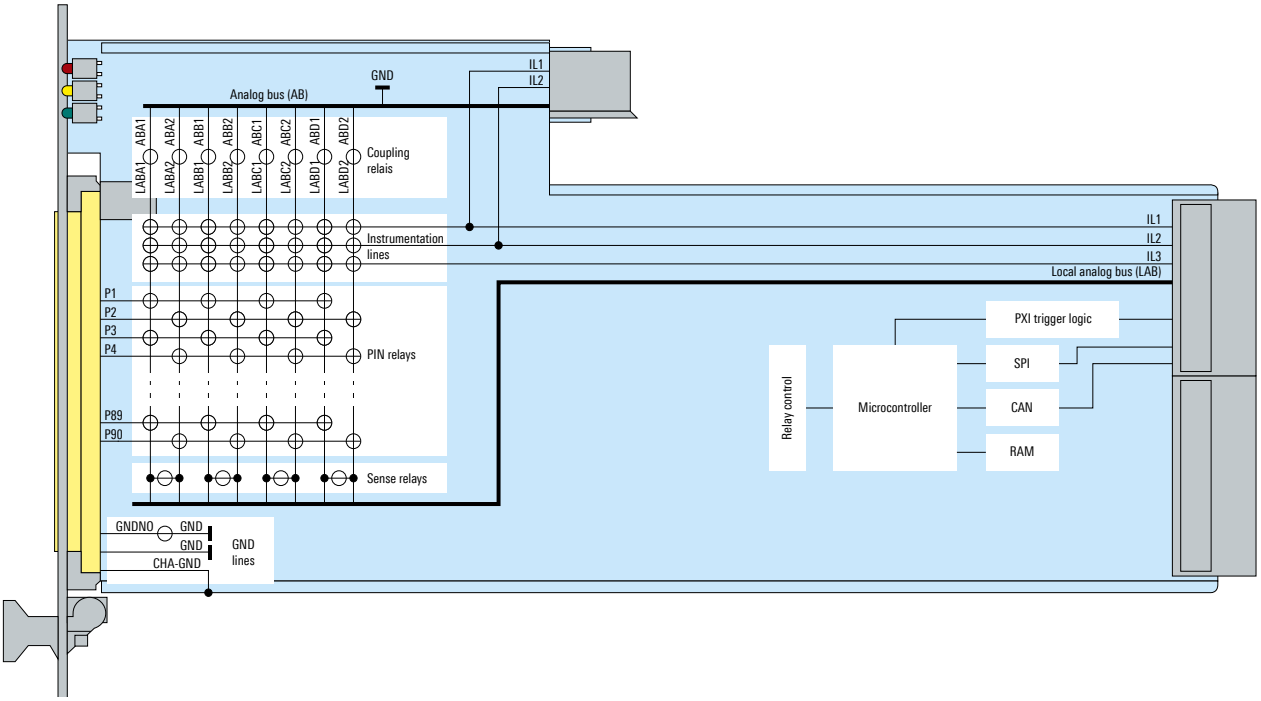
In highly complex test cases, the combined use of all modules yields a highly sophisticated virtual instrument. The R&S®TSVP backplane links the different modules together with CAN, cPCI and PXI buses. The analog measurement backplane is separated from the digital backplane to provide high-quality and reproducible analog signal routing.

Parallel components in a DUT circuit and test system residuals are compensated for by using guarding, sensing and phase-correct measurement technology.

Functional block diagram of the R&S®TS-PICT in-circuit test (ICT) extension module



Functional block diagram of the R&S®TS-PMB switching matrix module



Software

ICT programs are generated automatically by the automatic test generator (ATG), which creates a test proposal in XML format directly from the CAD data interface (BDL file format).

The well-structured graphical user interface, which is highly intuitive for anyone with experience in Windows based applications, makes debugging and optimization quick and easy.

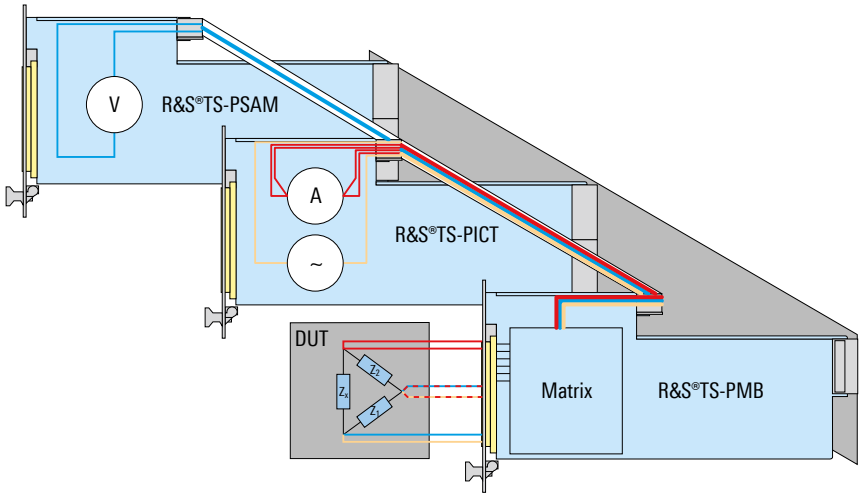
The high-speed tests, typically only 3 ms per part, are performed using a special precompiling algorithm of the EGTSL. This algorithm analyzes the test sequence and generates very efficient metacode when saving the program (e.g. optimization of range switches, selection of bus lines).

The simple execution of the ICT runtime via DLL calls from any sequencer software ensures flexible and straightforward integration into the software environment. The ICT program is implemented in the FCT like a normal test step.

Automated test generation

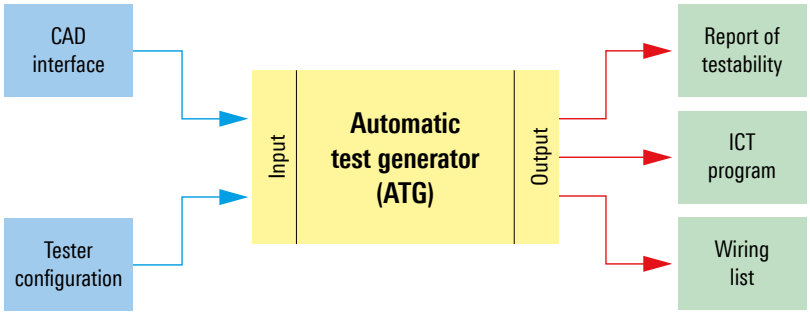
ICT programs are generated automatically by the automatic test generator (ATG). The ATG analyzes the DUT circuit described in CAD data (BDL file format). Appropriate test and guard points are selected automatically. Test requirements and available tester configurations are compared, and resulting testability problems are reported. An executable ICT program that can be run by EGTSL is generated. The wiring of the DUT can be started immediately using the wiring file that has been created.

Schematic diagram of a guarded impedance test



Flow chart of the ICT program generation

Program generation by the automatic test generator (ATG)



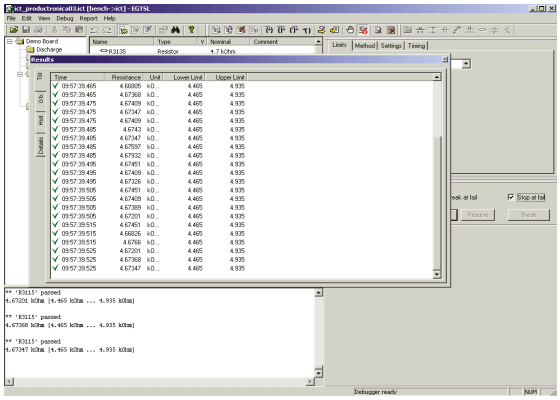
Debugging environment

The EGTSL debugging environment has the familiar look of modern Windows applications. With this graphical user interface, virtually anyone can quickly master the full spectrum of functionality and settings provided by EGTSL. There is no need to learn a special programming language or work with a predefined screen layout. Test engineers can create their own desktop and display all required information on one screen. They can scale, move and display the windows as needed.

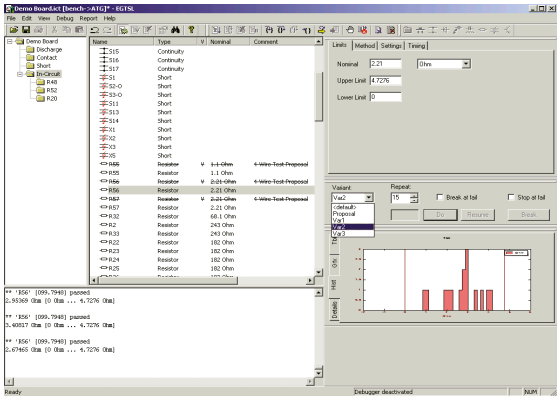
Even implementing a new test step is like creating a new folder in Windows Explorer, whose tree structure is similar to the ICT program flow in EGTSL.

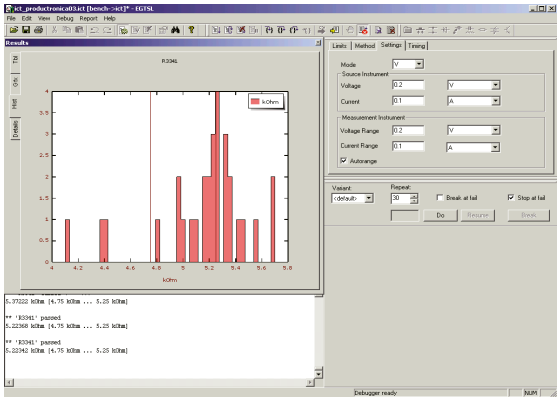
Within the EGTSL debugging environment, users can do the following:

- Create, delete or move test steps by a mouse click or drag & drop
- Change settings of test steps, e.g. limits, test method, stimuli and measurement
- Define specific timing models
- Use debugger functionalities such as setting breakpoints, step into or over certain test steps
- Define and handle different variants
- Export and import limits
- Use statistical tools such as histograms to verify stable results
- Display a detailed test report
- Create the core program for the panel test



EGTSL debugging environment





Execution/runtime

A separate sequencing program for the ICT option from Rohde&Schwarz is not needed. The ICT runtime can directly handle the customer's sequencer software, already used in the FCT.

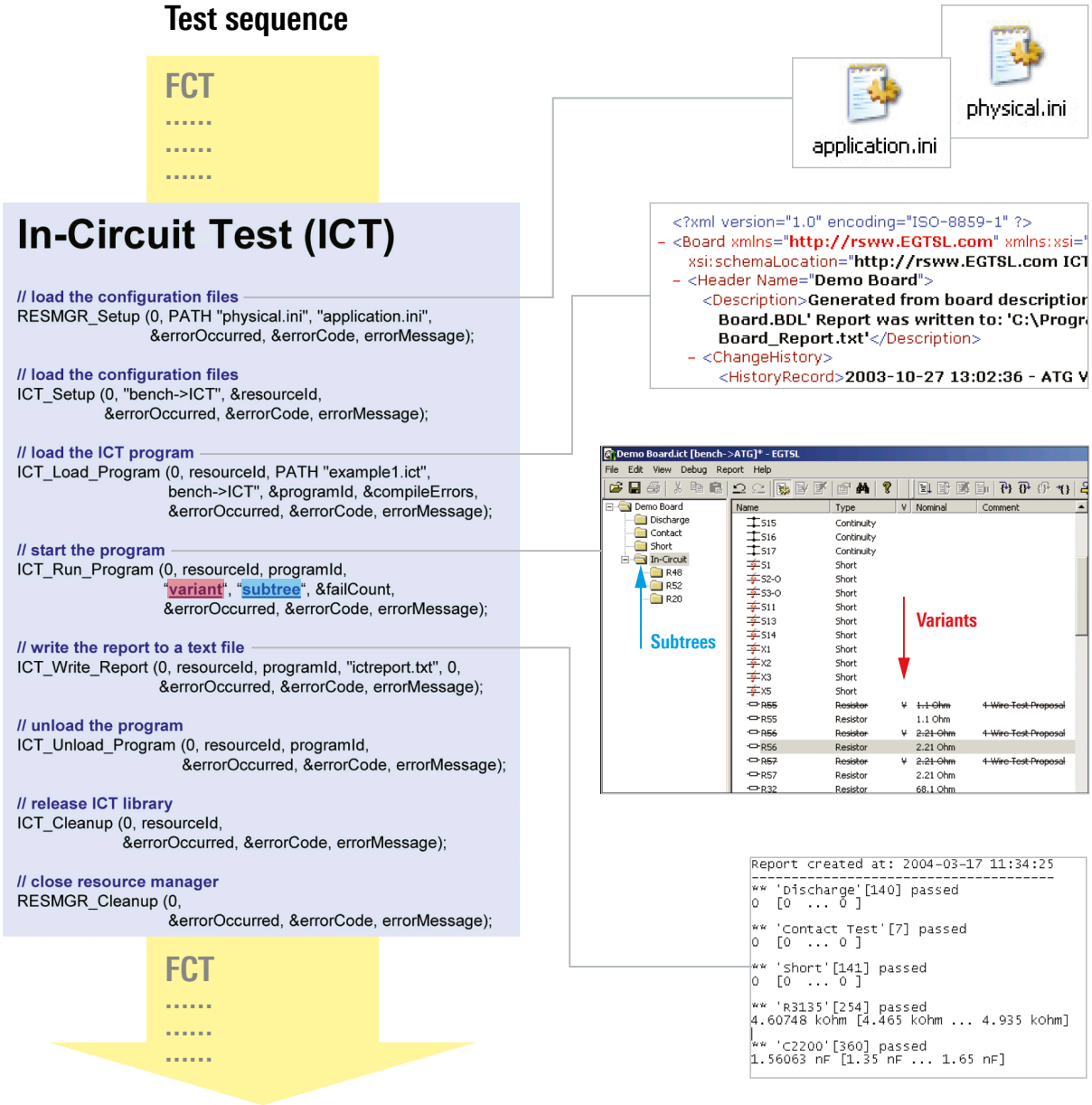
The ICT is executed by a DLL call from the test sequencer (e.g. off-the-shelf test sequencer or dedicated executable software).

The test hardware is automatically managed by the resource manager, which handles the information available in the tester configuration files (PHYSICAL.INI and APPLICATION.INI).

Special failure routines or variant settings are covered by the entire functionality of the sequencing program. Therefore, each time a DLL call is performed, variants defined in the ICT program can be selected and each subtree can be executed independently.

A complete test result containing the information of the ICT and FCT can be generated by the sequencer due to handover of the ICT failure count. Additionally, a detailed ICT report can be generated.

ICT program integrated into a functional test



Configurations

A single-chassis R&S®CompactTSVP can be configured with up to 990 test pins (11 R&S®TS-PMB modules). A dual-chassis configuration can provide additional 1440 test pins with up to 16 R&S®TS-PMB switching matrix modules in the R&S®PowerTSVP, yielding a maximum of 2430 test pins.

Several test system configurations are possible:

- "One box" ICT with up to 990 test pins and classic analog ICT functionality
- "One box" FCT/ICT solution with a mixture of FCT and ICT modules
- Dual-chassis FCT/ICT test system with measurement modules in the base unit and switching modules in the R&S®PowerTSVP; DUT fixturing via the R&S®PowerTSVP
- Dual-chassis ICT with up to 2430 pins and full analog ICT functionality

For all dual-chassis configurations, the devices have to be connected via the R&S®TS-PK01 analog measurement bus extension cable and the R&S®TS-PK02 CAN bus control cable.

Test fixture accessories

To accelerate integration of the R&S®TSVP into production test environments in a quick and cost-effective manner, an entire set of mass-interconnection support products has been created. The platform modules are equipped with a 96-pin DIN 41612 connector which is easy to handle in fixture wiring using wire-wrap techniques.

The interface between the R&S®TS-PAD3 receiver frame and the R&S®TS-F3F fixture frame is provided by the modular R&S®TS-PAX1 connector carriers on the test instrument side and the R&S®TS-F3X1 connector carriers on the fixture side. Optional, spring-loaded precision contacts can be mounted.

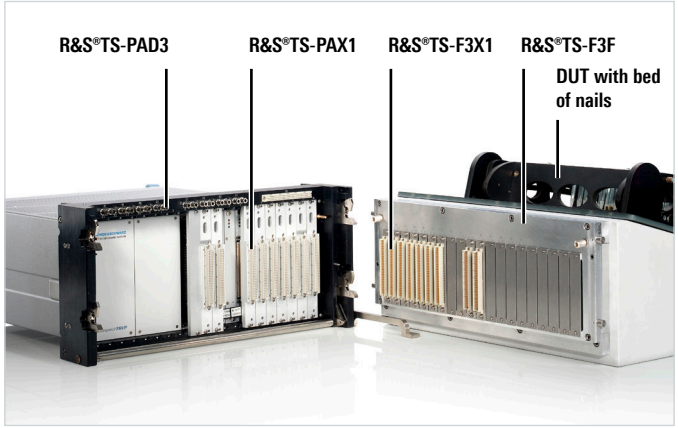
Security through self-test and diagnostic features

The built-in self-test capabilities range from fast diagnostics to complete, automated evaluations of all relays and switch paths. The use of the R&S®TS-PSAM allows a fast and comprehensive "in-system" self-test to be performed.

Diagnostic LEDs on the module front panel speed up installation and immediately indicate proper operation.

Combination of the R&S®PowerTSVP and R&S®CompactTSVP to form a fully analog ICT with 2430 pins

Test fixture accessories



SPECIFICATIONS

Application in R&S®CompactTSVP/R&S®PowerTSVP		
R&S®CompactTSVP		► 1 slot for R&S®TS-PSAM ► 1 slot for R&S®TS-PICT ► 1 slot for R&S®TS-PSU ► up to 11 slots for R&S®TS-PMB
R&S®PowerTSVP (optional)		up to 16 slots for R&S®TS-PMB
Interface		
DUT connector (front)		DIN 41612, 96 pins on R&S®TS-PSAM, R&S®TS-PMB
Tolerances of specified values apply under the following conditions:		
Recommended calibration period		1 year
Temperature range		+23 °C ±5 °C
Additional error specified by the temperature coefficient in the range		+5 °C to +18 °C and +28 °C to +40 °C

Resistor tests (DC)

Resistor test, non-guarded (R&S®TS-PSAM)

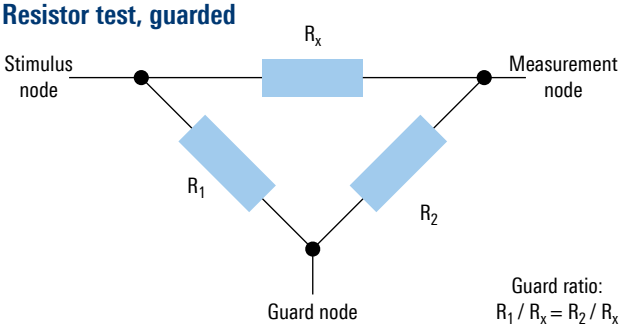
Range	Error limit	Source voltage (minimum)	Source current (minimum)	Mode [1]	Wires	Average	Sample interval
0.1 Ω to 1 Ω	1.0 + 5.0 mΩ [2]	0.5 V	100 mA	C	4	20	1 ms
1 Ω to 10 Ω	1.5 [3]	0.2 V	10 mA	C	4	20	1 ms
10 Ω to 100 Ω	0.5 [3]	0.2 V	25 mA	V	4		
100 Ω to 1 kΩ	0.5 [3]	0.2 V	2.5 mA	V	4		
1 kΩ to 10 kΩ	0.5 [3]	0.2 V	1.0 mA	V	2		
10 kΩ to 100 kΩ	1.0 [3]	0.2 V	0.1 mA	V	2	100	5 µs
100 kΩ to 1 MΩ	1.0 [3]	1.0 V	0.1 mA	V	2	20	1 ms
1 MΩ to 10 MΩ	1.0 [3]	5.0 V	0.1 mA	V	2	20	1 ms

Resistor test, guarded (R&S®TS-PSAM, R&S®TS-PICT)

Guard ratio (R_1:R_x, R_2:R_x)	Error limit [3]	Range (R_1 and R_2)	Source	Mode [4]	Wires
1:1	0.5	10 Ω to 100 Ω	0.2 V	V	6
1:10	1.0	10 Ω to 100 Ω	0.2 V	V	6
1:100	1.0	10 Ω to 100 Ω	1.0 V	V	6
1:1000	7.0	10 Ω to 100 Ω	1.0 V	V	6
1:1	0.5	100 Ω to 1 kΩ	0.2 V	V	6
1:10	0.5	100 Ω to 1 kΩ	0.2 V	V	6
1:100	1.0	100 Ω to 1 kΩ	1.0 V	V	6
1:1000	7.0	100 Ω to 1 kΩ	1.0 V	V	6

[1] C = current injection, voltage measurement. V = voltage injection, current measurement.
[2] Error limit: ±(% of reading + absolute value). Temperature coefficient: ±(0.1 × accuracy)/°C.
[3] Error limit: ± % of reading. Temperature coefficient: ±(0.1 × accuracy)/°C.
[4] V = voltage injection, current measurement.

Resistor test, guarded



Impedance tests (AC)

(R&S®TS-PSAM, R&S®TS-PICT)

Notes: The system residuals caused by the test system and the wiring in the fixture must be taken into account for all impedance measurements. Especially the parasitic capacitance has an influence on the measurement of large resistors, large inductors and small capacitors at a high frequency. The major part of the capacitance is compensated for by a software correction process that considers the actual system configuration. The remaining deviation (typically 0 pF to 30 pF) must be taken into account dependent on the actual interface connection with the DUT.
The error limits are increased to factor 2 in the case of stimulation with offset.
The error limits for capacitance and inductance are valid for a figure of merit ≥ 6, i.e. for a phase angle in the range of ±(90° ±10°).

Resistor test AC (non-guarded)				
	Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2]**
Measurement frequency 100 Hz	1 Ω to 6 Ω	1.2	0.2 V	V 4-wire
	6 Ω to 60 kΩ	0.7	0.2 V	V 4-wire up to 100 Ω
	60 kΩ to 300 kΩ	1.2	0.2 V	V
	300 kΩ to 1 MΩ	1.2	1.0 V	V
Measurement frequency 1 kHz	1 Ω to 6 Ω	1.2	0.2 V	V 4-wire
	6 Ω to 60 kΩ	0.7	0.2 V	V 4-wire up to 100 Ω
	60 kΩ to 300 kΩ	1.2	0.2 V	V
	300 kΩ to 1 MΩ	1.2	1.0 V	V
Measurement frequency 10 kHz	3 Ω to 20 kΩ	1.2	0.2 V	V 4-wire up to 100 Ω
	20 kΩ to 100 kΩ	2.2	0.2 V	V [3]

Capacitor test (non-guarded)				
	Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2]**
Measurement frequency 100 Hz	1 nF to 20 nF	1.0	U: 1.0 V	V
	6 nF to 100 nF	1.2	U: 0.2 V	V
	0.1 µF to 200 µF	0.7	U: 0.2 V	V 4-wire for ≥100 µF
	200 µF to 1000 µF	2.0	U: 0.2 V	V 4-wire
	1000 µF to 10000 µF	5.0	U: 0.2 V	V 4-wire
Measurement frequency 1 kHz	100 pF to 1000 pF	1.2 + 2.0 pF [4]	1.0 V	V
	0.6 nF to 10 nF	1.2 + 2.0 pF [4]	0.2 V	V
	0.01 µF to 1 µF	0.7 [1]	0.2 V	V
	1 µF to 10 µF	1.0 [1]	0.2 V	V
Measurement frequency 10 kHz	10 pF to 220 pF	1.0 + 2.0 pF [4]	1.0 V	V [3]
	220 pF to 1000 pF	0.7 + 1.0 pF [4]	1.0 V	V [3]
	1 nF to 22 nF	0.7 [1]	1.0 V	V
	60 pF to 1000 pF	1.0 + 2.0 pF [4]	0.2 V	V [3] average 5
	1 nF to 200 nF	1.2 [1]	0.2 V	V

Inductance test (non-guarded)				
	Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2, 5]**
Measurement frequency 100 Hz	1 mH to 20 mH	3.0	0.2 V	V
	20 mH to 30 H	2.0	0.2 V	V
	30 H to 100 H	5.0	0.2 V	V
Measurement frequency 1 kHz	250 µH to 2 mH	3.0	0.2 V	V
	2 mH to 3 H	2.0	0.2 V	V
	3 H to 10 H	2.0	0.2 V	V
Measurement frequency 10 kHz	60 µH to 1 H	2.0 [1]	1.0 V	V
	25 µH to 70 µH	2.0 + 1.0 µH [4]	0.2 V	V 4-wire
	70 µH to 50 mH	3.0 [1]	0.2 V	V

[1] Error limit: ±% of reading. Temperature coefficient: ±(0.1 × accuracy)/°C.
[2] V = voltage injection, current measurement.
[3] Min. current limit 20 µA.
[4] Error limit: ±(% of reading + absolute value). Temperature coefficient: ±(0.1 × accuracy)/°C.
[5] For 1 mH to 2 H: measurement delay = 0.4 × L [s/H]. For 2 H to 100 H: measurement delay = 1 s.

Contact test

R&S®TS-PSAM		
Source voltage		1 V to 5 V
Level		1 kΩ to 1 MΩ

Shorts/continuity test

R&S®TS-PSAM		
Source voltage		0.1 V to 0.5 V
Level		1 Ω to 1 kΩ

Discharge circuit

R&S®TS-PSAM		
Maximum input voltage		120 V
Maximum discharge current (typ.)	V > 13 V	10 mA
	V < 13 V	150 mA
	V < 7 V	300 mA
	V < 4.5 V	450 mA

Diode/transistor test

R&S®TS-PSAM, R&S®TS-PICT, R&S®TS-PSU or R&S®TS-PSU12		
Leakage current		0.1 µA to 100 mA
Forward voltage		0 V to 5 V
Zener voltage	for R&S®TS-PSU	–100 V to 100 V
	for R&S®TS-PSU12	–24 V to 24 V

Relay multiplexer

R&S®TS-PMB		
Number of pins per module		90
Number of pins per system		990 in base unit, 2430 in combination with R&S®PowerTSVP

ORDERING INFORMATION

Designation	Type	Order No.
Analog source and measurement module	R&S®TS-PSAM	1142.9503.02
In-circuit test (ICT) extension module	R&S®TS-PICT	1158.0000.02
Switching matrix module	R&S®TS-PMB	1143.0039.02
Power supply/load module	R&S®TS-PSU	1504.4530.02

Service that adds value

- Worldwide
- Local and personalized
- Customized and flexible
- Uncompromising quality
- Long-term dependability

Rohde&Schwarz

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- Energy efficiency and low emissions
- Longevity and optimized total cost of ownership

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